Total Dose Test Report for Samsung 4G NAND Flash Nonvolatile Memory

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I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the Samsung 4G NAND flash nonvolatile memory (part number K9F4G08U0A, Lot Date Code 625). This test was supported by the NASA Electronics Parts and Packaging (NEPP) Program.

II. Devices Tested

The Samsung NAND Flash Memory is a non-volatile memory that uses a floating gate NAND cell, implemented in 70 nm technology. It also provides a standard interface for pin and function drop-in compatibility. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. Detailed device information is provided in Table I. The parts have 4K blocks, a few of which can be "bad," as identified by the manufacturer. The blocks are 128Kx8, with 64 pages, 2Kx8. In this case, eight samples were irradiated, all of which had some bad blocks. There was also one unirradiated control device. The parts have a nominal 3.3 V power supply, plus an internal charge pump to generate higher voltages for writing and erasing.

Generic Part Number:	
Full Part Number	K9F4G08U0A
Manufacturer:	Samsung
Lot Date Code (LDC):	625
Quantity Tested:	9
Serial Numbers of Control Sample:	9
Serial Numbers of Radiation Samples:	1,2, 3, 4, 5,6,7,8
Part Function:	NAND Flash Memory
Part Technology:	CMOS
Case Markings:	Samsung 625 K9F4G08U0A PCB0 FHEE62AX
Package Style:	48 pin TSOP
Test Equipment:	Power Supply (+3.3V) Digital test board. Multimeters
Test Engineer:	M. Friendlich
Dose Levels (krad (Si)):	10, 20, 30, 50, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure.
Target dose rate (rad (Si)/min):	1200-1800

Table I. Device information

III. Test Facility

Testing was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Four parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other four parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed, then the next block, and so on until the entire memory is completed. A block diagram of the test apparatus is shown in Fig. 1.

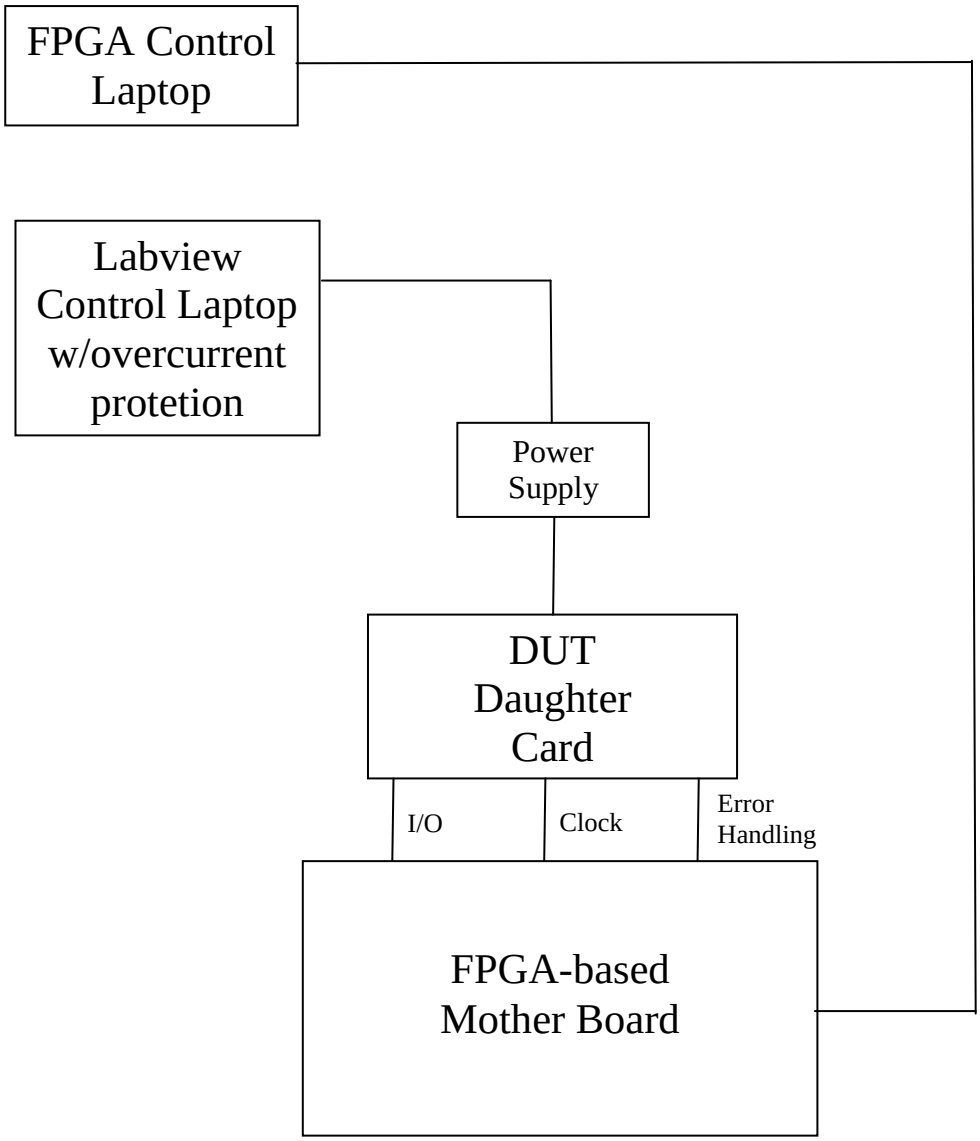

Fig. 1. Block diagram of the flash memory test apparatus.

V. Results

DUTs 1-4 were tested in read-only mode, while DUTs 5-8 were exercised in all the test patterns and the dynamic mode, as described above. All the DUTs had some bad blocks. At the 10, 20, and 30, 50, 75, and 100 krad (SiO_2) exposure levels, there were no errors in any device, in any test mode, except those identified in the bad blocks prior to irradiation, with three exceptions. First, DUT 5, after 75 krads(SiO_2), had three errors which were reset successfully, and which did not repeat in the next exposure. DUT 5 failed between 100 and 125 krads(SiO_2), due to failure of the erase circuit. Second, three of the read-only DUTs had errors after 75 krads(SiO_2). These were reset successfully and did not recur. Starting at 75 krads(SiO_2), the DUTs that were subject to the so-called dynamic SEU mode had errors, but only in that test mode. We will discuss these errors further, below. The other seven devices had no new errors at 125 or 150 krads(SiO_2), but they all failed at 200 krads(SiO_2). The DUTs that were cycled passed the initial read test, but they could not be erased. The four DUTs that were read only had an increase in the number of pre-rad errors. When we tried to reset these, the erase operation also failed. Leakage current was monitored throughout the test. Total current during exposure was 30 mA initially, for all eight samples, or an average of about 4 mA each. This current level, 4 mA per device, was confirmed for each device, when they were tested individually. At the end of the test, when the devices failed, leakage current had not increased for any device.

The dynamic SEU test mode is called that because it was developed for testing the read/erase/write operations with the heavy ion beam on. We use it in a TID test, without the beam on, because it sometimes reveals errors not found with any of our other test modes. In this test mode, each block is read and compared to an "expected" pattern, which is the complement of the actual pattern. Every bit is detected as an error, which is erased and reset. This procedure is repeated for each successive block, until the whole memory is completed. In one previous test, the manufacturer helped in the failure analysis, and found that some of the word lines were coupled together after a certain accumulated dose, which had the effect of erasing or partially erasing blocks that were not supposed to be erased. Something similar seems to be happening in these Samsung parts, starting at 75 krads(SiO_2), except that only block zero is ever affected. These parts all had a few bad blocks pre-rad, which had to be screened out. If one more block, block zero, were screened out, it would appear to be a simple work-around for this problem.

These parts were stored, unbiased, on a work-bench for a few days following the test. They were checked for annealing, between 100 and 120 hours, and all the parts were found to be fully functional again. The one exception to this was that the dynamic SEU test mode still produced errors in block zero, in all eight DUTs. The significance of the annealing is that the parts could probably operate in a space environment to much higher doses than those reported here. In a low dose rate space environment, the TID damage would anneal about as fast as it was created, and the parts might operate without degradation to very high doses.